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METHOD OF QUALITATIVE EVALUATION OF CENTRAL PROCESSOR UNIT EFFICIENCY OF SPECIAL PURPOSE SYSTEMS

Abstract. The proposed method of qualitative evaluation of central processor unit efficiency by visualizing the sign model and distribution histograms according to the microarchitecture of the central processor unit (CPU) for different manufacturers.

The method includes: creation of a relational model of a set of CPUs on many parameters, construction of histograms of distribution according to their main technical parameters according to microarchitecture for each firm of a manufacturer of a certain set, development of object-invariant quality criteria and construction of a sign model of dependence of the proposed criteria.

Visualization of the proposed criteria accelerates the process of determining the best CPU model of the respective firm across multiple parameters at the same time.

Keywords: central processors, microarchitecture, technical parameters, technological process, command pipeline, object-invariant criteria.

I. Introduction

Topicality. Implementation of modern projects for the creation of telecommunications, computer games, speech recognition, processing, compression and transmission of large-format video, archiving, etc. requires rapid arithmetic and logical operations, which are specified by the CPU management program to coordinate the work of all devices included in the composition of the computing complex.

Modern CPUs contain multiple cores in one body, they are multi-core. Multiple

kernels make it easy to perform concurrent tasks at the same time, which can significantly increase the speed of computer programs when properly optimized. Multicore is the most promising way to increase the efficiency of both the CPU and the computing complex as a whole. To this end, technologies are sometimes used to create multiple virtual cores from one physical core. However, increasing the number of cores does not lead to a proportional increase in processor efficiency, and in some cases even worse than the single-core variant is possible. It all depends on the ability to perform a specific task in several parallel threads and on the high-quality implementation of multicore support for specific software.

Many works of V.D. Baykova, VI Korniychuk, V.D. Puzankova, K.G. Samofalova, V.B. Smolova, VP Tarasenko, Steve Furber, Borut Robic, Jurij Silc, Theo Ungerer, Reinhold P. Weicker and others dedicated to the use of CPUs, but insufficiently clarified the issue of accelerating the procedure of analysis of multiple CPUs on many basic technical parameters at the same time and determining the best model of the respective company manufacturer [1-5].

Determining the best or industry-leading CPU application requires a lot of time and energy because it requires simultaneous consideration of combinations of many parameters of modern CPU models from different manufacturers.

Therefore, the development of a method of qualitative evaluation of CPU performance, which will speed up the process of determining the best or finding the required model of the CPU model of the respective company of the manufacturer by many parameters at the same time is an urgent task.

II. Problem statement

The purpose of this work is to increase the efficiency of microprocessor systems by developing a method of determining the best existing modern models of CPUs simultaneously on many parameters due to the creation of a relational model of multiple CPUs on many basic technical parameters, the construction of character models of distribution by basic characteristics, quality criteria and visualization of the constructed sign model of dependence of the proposed criteria. To achieve this goal in the direction of analyzing the performance of the CPU, which will speed up the process of determining the best model of the CPU of the respective company on many parameters simultaneously, it is necessary to solve the following sequence of tasks:

 conduct systematic analysis of existing CPUs and to determine, on the basis of the heuristic method, the main technical parameters that directly affect the performance of the CPU;

- create a relational model of multiple CPUs with structured basic technical parameters;

create a mathematical model to determine the relationship between the main technical parameters;

- determine the type of modeling and develop object-invariant conditional quality criteria for the CPU;

 build distribution histograms according to the main technical parameters according to the microarchitecture for each manufacturer;

- develop a sign model of the dependence of the quality criteria of the CPU.

III. Results

Based on the heuristic, a set of modern CPU models was proposed and the main technical parameters directly influencing CPU efficiency were proposed, a relational model of the CPU set was created according to the corresponding structured data of selected technical parameters [5–11] of different manufacturers, which are given in Table 1.

Table 1

Relational model of CPUs of different companies with basic technical parameters

Nº	Companies	Nº	CDU	G	M	Quality criteria	
(Companies)	(Chipset)	(CPU)	CPU	3	M, nm	K_S	K_M
1	ARM	1	Cortex-A8	13	40	0.46	0.75
		2	Cortex-A15	15	32		

N₂ (Companies)	Companies (Chipset)	N₂ (CPU)	CPU	S	M, nm	Quality criteria	
						K_S	K_M
1	ARM	3	Cortex-A53	8	28	0.46	0.75
		4	Cortex-A57	15	20		
		5	Cortex-A72	15	16		
		6	Cortex-A55	8	10		
		7	Cortex-A75	13	10		
2	Qualcomm (Snapdragon)	1	Scorpion	12	40	0.38	0.75
		2	Krait	11	28		
		3	Kryo 1	8	14		
		4	Kryo 2	12	10		
		5	Kryo 3	13	10		
3	Samsung (Exynos)	1	M1/M2 (Mongoose)	13	14	0.13	0.28
		2	M3 (Meerkat)	15	10		
4	Nvidia	1	Denver	15	28	0.13	0.42
		2	Denver 2	13	16		
5	Apple (Ax)	1	Typhoon	14	20	0.12	0.50
		2	Twister	16	14		
		3	Hurricane	16	10		

Continuation of Table 1

Note: S – the number of stages of the pipeline command CPU, M – technological process, K_S , K_M – quality criteria for the number of stages of the conveyor and the technological process of different manufacturers, respectively.

One indicator of CPU efficiency is the number of stages of a computational command pipeline. For each company the manufacturer is offered a corresponding histogram, which is presented in Fig. 1, a.

The value of the applied technological process is determined and the corresponding histogram is presented for each firm to the manufacturer, which is presented in Fig. 1, b.

To determine the quality criteria, you need to know the maximum and minimum values of the CPU parameters for each firm, respectively. Then S_{min} , S_{max} and M_{min} , M_{max} – the minimum and maximum value of the number of stages of the conveyor and the process of different manufacturers.

To determine the relationship between the parameters, we have a generalized mathematical model that takes the form

$$F(S_{min}, S_{max}, M_{min}, M_{max}).$$
(1)

Taking into account the absence of analytical dependence (1), conditional modeling is chosen between the determined parameters.



Figure 1. Distribution histograms according to the microarchitecture of the CPUs the respective manufacturer's firm: a) – by the number of stages; b) – by technological process.

Note:

the numbers 1, 2, ..., 7 correspond to the serial number of the microarchitecture of the CPU of the respective firm of the manufacturer (Table 1).

The following object-invariant quality criteria and their physical interpretation have been developed on the basis of the properties of the theory of dimensionality of structured data (Table 1) and the heuristic method:

– the value characterizing the range of the number of stages of the pipeline commands of the CPU commands, preferably at $K_S \rightarrow 1$:

$$K_{S} = \frac{S_{max} - S_{min}}{S_{max}};$$

– the value that characterizes the range of values of the CPU used, is better at $K_M \rightarrow 1$.

$$K_M = \frac{M_{max} - M_{min}}{M_{max}}$$

The created criterion equation is as follows

$$\Psi\left(\frac{S_{max}-S_{min}}{S_{max}}; \frac{M_{max}-M_{min}}{M_{max}}\right) = 0.$$

Based on the π - theorem and properties of algebra of sets the sign model of dependence of multiparametric quality criteria of the CPU, represented in the form of universal set, is constructed *K* in Fig. 2 for the range of the number of stages of the pipeline commands and technological process.



Figure 2. A sign model of the dependence of CPUs quality criteria in dimensionless coordinates by the number of stages of the conveyor team and the process

Note: the numbers 1, 2, ... 5 correspond to the serial number of the companies of CPU manufacturers (Table 1).

Venn diagrams are used to accelerate the analysis, dividing the plural K to subsets {A, B, C, D }.

The best geometric space for the set *K* is the intersection of subsets $B \cap C$, to which the firm belongs ARM and Qualcomm. These architectures have the best value of the process used in the line of processors considered and the optimal number of stages of the pipeline commands.

To the geometric space of intersection of sets $A \cap D$, to which the firm belong Samsung. The geometric space of intersection of sets $A \cap C$ contains CPUs manufactured by Nvidia and Apple.

IV. Conclusions

The important scientific and technical problem of increasing the speed of the procedure of determining the best model of the CPU is solved in the work of the respective firm by many technical parameters at the same time due to the development of a method of qualitative evaluation of the effectiveness of the CPU, the sequence of which involves:

1. Determination of the list of the main technical parameters that directly affect CPU performance based on the heuristic method.

2. Creating a relational model of a plurality of CPUs with structured technical parameters that significantly influence the choice of a device manufacturer.

3. Construction of histograms of the distribution of CPU microarchitectures of the respective CPU manufacturer according to the technological process and the number of stages of the pipeline of teams, visualization of which allows to determine the best CPU models according to the microarchitecture of a specific manufacturer firm.

4. Construction of a generalized mathematical model of the relationship between the main technical parameters.

5. Development of object-invariant conditional criteria of quality of the CPU on many basic technical parameters simultaneously on the basis of properties of the theory of dimensions.

6. Development of a sign model of the dependence of these criteria on the universal plane, the visualization of which helped to accelerate the procedure of geometric interpretation of Venn diagrams and to determine the best models of the CPU.

Among the many modern CPUs under study, the most effective models found by ARM and Qualcomm were identified.

In the future, it is advisable to conduct a systematic analysis of modern CPU models of various manufacturers, which are the most used in a particular industry, by their productivity.

References

1. Полетаев С. А. Параллельные вычисления на графических процессорах. – Режим доступа : <u>http://www.iis.nsk.su/files/articles/sbor_kas_16_poletaev.pdf</u>.

2. Сергиенко А. М. Микропроцессорные устройства на программируемых логических ИС / С. А. Сергиенко, В. И. Корнейчук. – К : «Корнійчук», 2005.

3. Borut Robic. Processor Architecture: From Dataflow to Superscalar and Beyond / Robic Borut, Silc Jurij, Ungerer Theo. – Springer, 1999.

4. Steve Furber. ARM System-on-Chip Architecture (2nd Edition) / Furber Steve. – Addison-Wesley Professional, 2000.

5. Знакові моделі структурованих залежностей динамічного розвитку співпроцесорів / А. Г. Лукашенко, І. А. Зубко, В. В. Корнух, В. А. Лукашенко, В. М. Лукашенко // Вісник ЧДТУ. – 2017. – С. 11–16.

6. Reinhold P. Weicker. 1984. Dhrystone: a synthetic systems programming benchmark // Communications of the ACM. – 1984. – Vol. 27. – Issue 10. – P. 1013–1030. doi: 10.1145/358274.358283.

7. Конвеєр команд. – Режим доступа : <u>https://uk.wikipedia.org/wiki/</u> Конвеєр команд.

8. ARMarchitecture. –Режимдоступа :https://en.wikipedia.org/wiki/ARM_architecture.

9. ListofARMmicroarchitectures.Режимдоступа:https://en.wikipedia.org/wiki/List_of_ARM_microarchitectures.

10. ComparisonofARMcores. –Режимдоступа :https://en.wikipedia.org/wiki/Comparison_of_ARM_cores.

11. ListofARMmicroarchitectures.Режимдоступа :https://en.wikipedia.org/wiki/List_of_ARM_microarchitectures.