BULLETIN of Cherkasy State Technological University

Journal homepage: https://bulletin-chstu.com.ua/en

Vol. 30 No. 2. 2025

UDC 621.316
DOI: 10.62660/bcstu/2.2025.53

Broadband high-linearity voltage buffer with enhanced load-driving capability

Oleksiy Azarov*
Doctor of Technical Sciences, Professor
Vinnytsia National Technical University
21021, 95 Khmelnytske Shose Str., Vinnytsia, Ukraine
https://orcid.org/0000-0002-8501-1379

Serhii Bohomolov
PhD in Technical Sciences, Associate Professor
Vinnytsia National Technical University
21021, 95 Khmelnytske Shose Str., Vinnytsia, Ukraine
https://orcid.org/0009-0003-3823-8380

Oleksandr Lukashuk
Postgraduate Student
Vinnytsia National Technical University
21021, 95 Khmelnytske Shose Str., Vinnytsia, Ukraine
https://orcid.org/0009-0002-7485-1193

Abstract. The development of buffer cascades with high linearity, wide bandwidth, and the ability to work with low-impedance or capacitive loads is a pressing issue in modern analogue electronics. The aim of this work was to create a broadband, high-linearity voltage buffer with increased load capacity for use in high-precision systems. The study used computer modelling to analyse the electrical parameters of the proposed cascade and compared it with traditional circuits. A new circuit design approach to building a buffer cascade is proposed, based on an optimised output stage structure and a combination of cascode and push-pull topologies. This configuration reduces output resistance, minimises nonlinear distortion and ensures high signal transmission stability. Modelling results confirmed that the developed buffer has an extended bandwidth, improved frequency characteristics and reduced harmonic distortion over a wide frequency range. In particular, when working with high-capacity loads (up to 200 pF), a significant reduction in signal delay (up to 80-90%) was observed compared to conventional complementary metal-oxide-semiconductor implementations. The assessment of the influence of active element parameters on dynamic stability also confirmed the high reliability of the device under variable load conditions. The research results can be used to improve the performance of analogue-to-digital converters, drivers, amplifiers and control circuits operating in modes with increased current load. The practical value of the development lies in its ability to be integrated into high-precision, energy-efficient and high-speed electronic systems that require stable operation of the buffer cascade under complex load conditions

Keywords: high load; high precision; buffer device; cascode cascade; push-pull structure

Article's History: Received: 18.01.2025; Revised: 30.04.2025; Accepted: 16.06.2025.

Suggested Citation:
Azarov, O., Bohomolov, S., & Lukashuk, O. (2025). Broadband high-linearity voltage buffer with enhanced load-driving capability. *Bulletin of Cherkasy State Technological University*, 30(2), 53-62. doi: 10.62660/bcstu/2.2025.53.

*Corresponding author

INTRODUCTION

Voltage buffer devices are key components in modern electronic systems, as they ensure effective signal matching between different circuit elements. They are widely used in analogue-to-digital and digital-to-analogue conversion channels, measuring systems, amplifiers, communication systems, and radio electronics, where it is necessary to "uncouple" a low-power input signal (voltage) generator from a low-impedance load or to form an output current within a specified range. One of the key requirements for buffer devices is to ensure minimal voltage loss during its transmission from input to output, which requires a high transmission coefficient accuracy, which should be as close to unity as possible. In addition, it is important to increase the load capacity, which improves the energy efficiency of the device and its resistance to changes in load parameters. At the same time, modern electronic systems impose strict requirements not only on load capacity, but also on the linearity of transmission characteristics and broadband capability. This is especially true for high-frequency and high-precision applications, where even minor non-linear distortions can significantly impair device performance. Traditional voltage buffer circuits often have limited bandwidth and non-linear characteristics, which reduces their effectiveness in such applications.

Traditional buffer cascades based on operational amplifiers have high input impedance and low output impedance, which allows for effective signal matching in analogue circuits (Patent No. 158284, 2025). However, their bandwidth is limited, making them less suitable for high-frequency applications. An important area of research is improving the linearity of buffer devices. In a study by O.D. Azarov & O.Y. Stahov (2022), an approach was proposed for creating highly linear push-pull voltage buffer device cores with parametric zero offset compensation. A method for the structural and functional organisation of a zero-offset current generator has also been developed, which allows the output current to be regulated. This will enable the device to be used in cases where a leakage current is required for the amplifier circuit. The study showed that the introduction of parametric compensation significantly (by tens of times or more) reduces zero offset and linearity errors while maintaining the required level of performance.

In modern research on broadband high-linearity voltage buffers, considerable attention was paid to achieving high speed, expanding the passband and improving the linearity of the transfer characteristics while maintaining high load capacity. A promising approach to achieving these goals is the use of adaptive current bias circuits, which reduce static power consumption and minimise nonlinear distortion, as reported by A. Chang & B. Kong (2020). For example, the use of cascode structures with adaptive current control during transient processes improved the stability and dynamic characteristics of buffers without significantly increasing the size of the chip. Such solutions provide high linearity and speed, making them suitable for high-speed analogue circuits with low-impedance loads.

The development of broadband high-linearity buffers focuses on reducing noise, improving common-mode rejection, and expanding the bandwidth. A promising solution for achieving these characteristics is the use of differential cascades with high input impedance and low noise, which ensure stable signal transmission even under variable load conditions, according to J. Liao *et al.* (2025). The implementation of such buffers with a fully differential architecture significantly reduces the input noise level and improves the common-mode rejection ratio while maintaining a wide frequency range. Such approaches provided high signal transmission accuracy and effective reduction of system noise, making them promising for high-precision analogue circuits.

Biomedical applications require the use of buffer amplifiers with low power consumption, low noise, and high gain for accurate reproduction of low-amplitude signals. One promising approach to meeting these requirements, as pointed out by S. Mythry & J. Moni (2019), is the use of bulk-driven folded cascode topologies, which ensure signal stability even at low supply voltages. The use of cascode structures with current mirrors, such as Wilson current mirrors, allowed for effective gain increase while minimising noise and power consumption. Such solutions, implemented on modern complementary metal-oxide-semiconductor technologies, demonstrated high stability and sensitivity, making them suitable for sensor systems and medical devices where measurement accuracy and energy efficiency are critical.

Dynamic amplifiers are increasingly used in modern analogue-to-digital converters due to their high energy efficiency and speed. However, their main drawback remains limited linearity, which can significantly affect the accuracy of signal conversion. To improve this parameter, linearisation methods are being developed, including one by B. Yang *et al.* (2025), which allow the nonlinear effects of input transistors to be compensated for, reducing harmonic distortion without significantly increasing power consumption. The use of such approaches in modern analogue-to-digital converter architectures significantly improves the signal-to-noise-distortion ratio, making them promising for high-precision and high-speed applications.

A number of important characteristics of traditional buffer devices, in particular limited bandwidth, insufficient linearity and low load capacity, complicate their use in high-frequency and high-precision applications. Despite existing approaches to compensation for distortions, the issues of stable buffer operation under variable load conditions and a wide frequency range remain open. This necessitates the development of a new approach to the construction of a broadband high-linearity voltage buffer with improved performance characteristics. The aim of the study was to develop a

broadband high-linearity voltage buffer with improved performance characteristics, in particular with reduced nonlinear distortion, increased voltage transfer coefficient to values close to unity, and high stability under various load conditions.

MATERIALS AND METHODS

The research methodology was aimed at developing a broadband high-line buffer device with increased load capacity that meets modern requirements for speed, accuracy and stability of operation. To achieve these goals, an approach was chosen that combines theoretical analysis, computer modelling and comparative analysis of the characteristics of the developed device with existing solutions. The first stage of the research was a detailed analysis of existing circuit solutions for buffer cascades, including cascode, push-pull and differential structures. A literature review was conducted to identify the key factors affecting the load capacity, linearity, stability, and frequency characteristics of buffers. This stage made it possible to formulate requirements for the developed circuit, taking into account current trends in analogue device circuitry. At the second stage, a mathematical model of the buffer device was developed, taking into account the main static and dynamic parameters of the circuit. For this purpose, modern software tools such as Micro Cap were used, which allow accurate simulation of electrical processes in complex analogue circuits. During the modelling, key parameters such as voltage transfer coefficient, input and output impedance, bandwidth, speed and harmonic distortion level were evaluated. This made it possible to analyse in detail the operation of the device under various load conditions and identify potential ways to improve it.

Based on the simulation results, an optimised buffer device circuit was synthesised, which provides increased load capacity, operational stability and a high voltage transfer coefficient. At the same time, various options for cascode and push-pull structures were implemented to improve the dynamic characteristics of the device and minimise nonlinear distortions. The final stage of the study was a comparison of the characteristics of the developed device with existing analogues. For this purpose, a comparative analysis was carried out, which included an assessment of such indicators as bandwidth, transmission coefficient, distortion level, load capacity, and energy efficiency. This made it possible to determine the advantages of the proposed method and outline possible areas of its practical application, including high-speed analogue-to-digital converters, low-distortion amplifiers, and signal transmission systems.

Methods of buffer voltage excitation. Voltage buffers were used to ensure compatibility between the input signal coming from a high-impedance source and the low-impedance input of the amplifier (they are also called voltage repeaters). They are characterised by a number of properties: their gain is equal to unity, they have high input impedance and low output impedance. Thanks to these characteristics, such devices are effectively used to match different circuit elements. In particular, buffer cascades were used to match the input of a high-line analogue-to-digital converter with a current or voltage signal source, as well as to match the output of a digital-to-analogue converter with a load.

This study used a precision buffer device implemented on the basis of a push-pull amplifier cascade with an operational amplifier in voltage repeater mode. This configuration allowed high signal transmission accuracy to be achieved thanks to deep feedback, which ensures minimal static scale and linearity distortions. To reduce the influence of output resistance and improve load capacity, a multi-stage structure with a high current transfer ratio was used, which significantly reduces transmission characteristic distortions even with large load changes.

The amplifier cascade was constructed using bipolar transistors, which provide the high gain and wide bandwidth required for high-speed applications (Rohde & Newkirk, 2000; Kim *et al.*, 2006). However, the basic voltage buffer circuit shown in Figure 1 had low load capacity, determined by the output resistance, which limited its effectiveness in high-load conditions (Patent No. 158284, 2025).

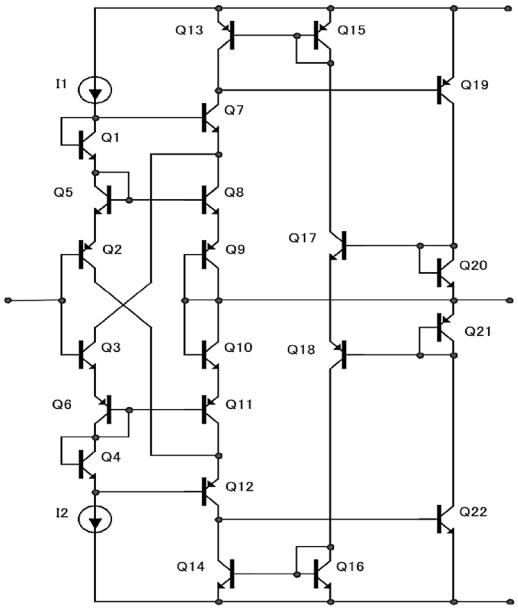

Figure 1. Schematic diagram of a simplified voltage buffer

Notes: Q – transistor; I – current source

Source: created by the authors based on Patent No. 158284 (2025)

To eliminate this drawback, a push-pull amplifier cascade was introduced, which significantly reduced the output resistance, improving the circuit's ability to operate with low-impedance loads and reducing nonlinear distortion. This solution stabilised the device's transmission characteristics, reduced power losses and improved overall performance, including increased signal transmission accuracy, improved frequency stability and reduced

distortion, which are critical for high-precision analogue circuits. At the same time, the output resistance:

$$r_{out} = r_e. \quad (1)$$

It determines how effectively the buffer transmits the signal from the source to the load without voltage loss or distortion. In electronics, the parameter r_e (emitter resistance) is a resistor connected between the emitter of a bipolar transistor and ground (or another reference potential) in an emitter follower circuit. It is key to analysing the operation of transistor amplifiers and performs several important functions that affect the stability and dynamic characteristics of the buffer. The emitter resistance was determined by the thermal potential and emitter current using the formula:

$$r_e = \frac{T_\varphi}{I_e}, \quad (2)$$

where $T_\varphi \approx 25$ mV (at room temperature) – thermal potential; I_e – emitter current (A). Thermal potential T_φ – is a physical parameter that characterises the effect of temperature on the operation of semiconductor components, in particular transistors. It played a key role in the formation of current in p-n junctions of transistors and determines the dependence of the electrical characteristics of the buffer on temperature. It is calculated as:

$$T_\varphi = \frac{kT}{q}, \quad (3)$$

where $k \approx 1.38 \times 10^{-23}$ J/K – Boltzmann constant; T – absolute temperature (in Kelvin); $q \approx 1.6 \times 10^{-19}$ C – electron charge. Calculation example – if the emitter current $I_e = 1$ mA, then:

$$r_e = \frac{25\ mV}{1\ mA} = 25\ ohms. \quad (4)$$

Thus, r_e is a dynamic resistance and depends on the emitter current. The greater I_e, the smaller r_e, which affects the amplifier parameters. The presence of output resistance in the circuit causes distortion of the transfer characteristic and a change in scale. To increase the load capacity and maintain the required linearity, a push-pull two-channel current amplifier was included in the circuit. The generalised structure of such a buffer device is shown in Figure 2 (Azarov & Stahov, 2022).

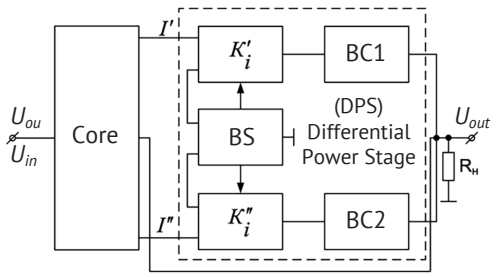

Figure 2. Functional diagram of a precision buffer device based on a push-pull symmetrical structure
Notes: U_{in} – input voltage; K_i' і K_i''– amplifying stages; BS – balancing scheme; BC1 і BC2 – current switches; U_{out} – output voltage
Source: created by the authors based on O.D. Azarov & O.Y. Stahov (2022)

The basis of this device is the core, which was also designed according to a push-pull circuit. The use of a push-pull amplifier for direct current helped to increase the load capacity while maintaining the established linearity of the core. It should be noted that it is the core that determines the potential characteristics of the entire system. At the same time, the error levels of individual elements can significantly depend on the specific implementation of the device core circuitry. The balancing circuit provided a proportional relationship between the transmission coefficients and equalises their values across the entire input signal range (Azarov & Stahov, 2022). To achieve self-balancing, the following condition must be met:

$$\frac{I'}{I_p} = \frac{I_p}{I''}, \quad (5)$$

where I_p – is the operating point current. In this case, the amplification coefficients must be equal to:

$$K_i' = K_i''. \quad (6)$$

In this case, to increase the load capacity and ensure the necessary linearity, a possible option is to introduce a push-pull amplifier cascade on transistors Q45 and Q46, as shown in diagram 2 (Fig. 3). The push-pull structure provided symmetrical signal transmission, minimising nonlinear distortion due to identical operating conditions for both halves of the cascade. It also allows for an increase in output current, which improves the cascade's ability to operate with low-impedance loads, improving signal transmission stability. Additionally, the push-pull circuit reduces the influence of thermal effects and improves the voltage transfer ratio, making it an effective solution for high-speed and high-linearity analogue devices.

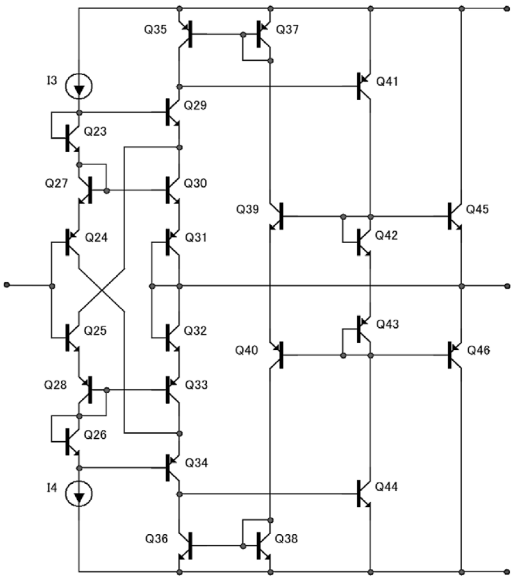

Figure 3. Schematic diagram of an improved voltage buffer
Notes: Q – transistor; I – current source
Source: created by the authors based on Patent No. 158284 (2025)

The addition of a push-pull amplifier stage (PAS) in the feedback loop between the amplifying core and the load makes it possible to reduce the output impedance to a value of:

$$r_{out} = \frac{r_e}{K_i}, \quad (7)$$

where K_i – total PAS amplification factor, calculated using the formula:

$$K_i = \frac{2K_i' K_i''}{K_i' + K_i''}. \quad (8)$$

This method ensured high accuracy and stability of the buffer device with minimal distortion, which is critical for high-speed analogue applications. This allows for effective signal matching between a low-power source and a low-impedance load, minimising power loss and ensuring high signal transmission linearity.

RESULTS AND DISCUSSION

The results of the study showed that the introduction of an amplifier cascade significantly improved the stability of the device's linearity when the load changed. As can be seen from Table 1, Circuit 1 shows a significant increase in linearity deviation with a decrease in load resistance, reaching almost 700 μV at a load of 1 kOhm. This indicates that at low resistance values, the output cascade without an amplifier loses its ability to maintain stable transfer characteristics, which can lead to significant signal distortion and reduced data transmission accuracy. At the same time, circuit 2, which uses a push-pull amplifier stage, demonstrates significantly better stability, maintaining a low level of linearity deviation even with a significant decrease in load resistance. The deviation index for this circuit varies only from 12.32 μV to 13.63 μV, which indicates the high efficiency of this solution for ensuring high signal transmission accuracy. This confirmed the feasibility of using amplifier stages to improve the load capacity of buffer devices, especially when working with low-impedance loads, which is critical for high-speed and high-line analogue circuits.

Table 1. Dependence of linearity deviation on load resistance

Load resistance, kOhm		None	10	5	2	1
Linearity deviation, μV	Circuit 1	12.47	40.15	80.71	256.59	697.93
	Circuit 2	12.32	12.58	12.63	13.02	13.63

Source: created by the authors

The graphs in Figure 4 show the dependence of transmission characteristic deviations for circuits without an amplifier cascade (a) and with an amplifier cascade (b). As can be seen, the introduction of an amplifier cascade significantly stabilised the circuit operation, reducing the level of nonlinear distortions. In the case of a circuit without an amplifier, a significant increase in deviation is observed when the input voltage changes, which can lead to a loss of signal transmission accuracy. At the same time, the circuit with an amplifier stage demonstrates more stable characteristics, maintaining a low level of distortion even with large changes in the input signal. This confirms the feasibility of using amplifier stages to ensure high signal transmission accuracy, especially under variable load conditions.

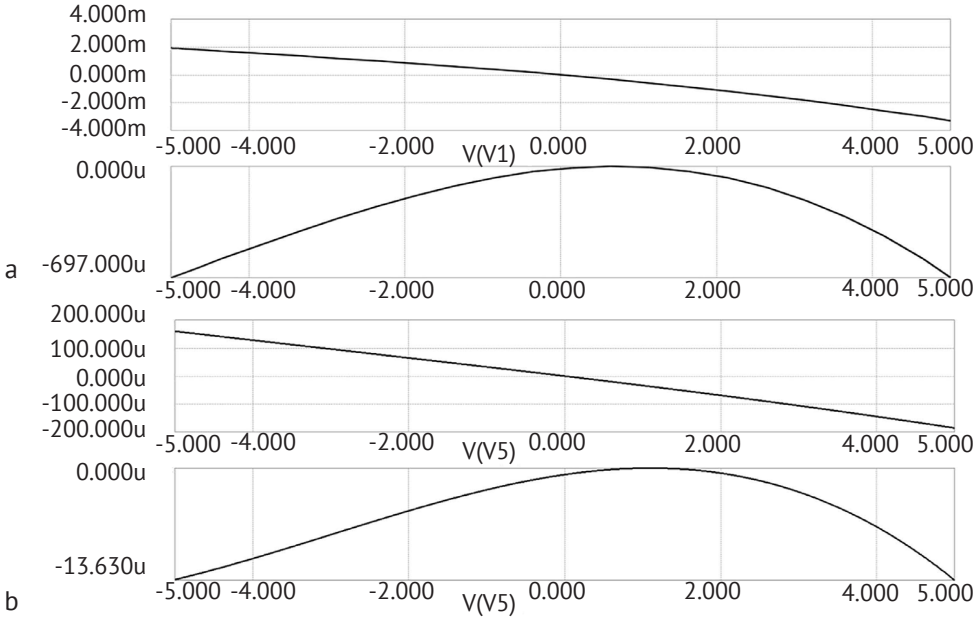

Figure 4. Transmission characteristic deviations

Notes: a – simple buffer device; b – improved buffer device

Source: developed by the authors as a result of modelling in Micro Cap

The amplitude-frequency characteristic was a critically important parameter in the design of voltage buffers, as it determined the device's ability to maintain a stable output signal at different input signal frequencies. In the case of voltage buffers, especially for broadband and high-line models, the amplitude-frequency characteristic is crucial for ensuring efficient operation at high frequencies, minimising distortion and maintaining linearity under heavy loads. One of the main tasks for broadband buffers was to maximise the bandwidth without significantly affecting linearity. This can be achieved by optimising circuit design solutions, such as the introduction of cascode or push-pull topologies, which help to reduce parasitic effects that limit the bandwidth. These approaches make it possible to maintain stable linearity even at high frequencies, which is critical for buffers operating with high loads.

High-linearity voltage buffers must ensure minimal distortion of the input signal over a wide frequency range. The linearity of the amplitude-frequency response is a key parameter because it affects the accuracy of signal reproduction. In voltage buffers, especially in high-precision applications, it is important that the amplitude-frequency response remains linear throughout the entire operating frequency range. This helps to avoid non-linear signal distortions such as harmonic distortion or changes in amplitude. In buffers with low linearity, there was a significant increase in the harmonic distortion coefficient with increasing frequency or input signal voltage. The amplitude-frequency characteristic graphs are shown in Figure 5.

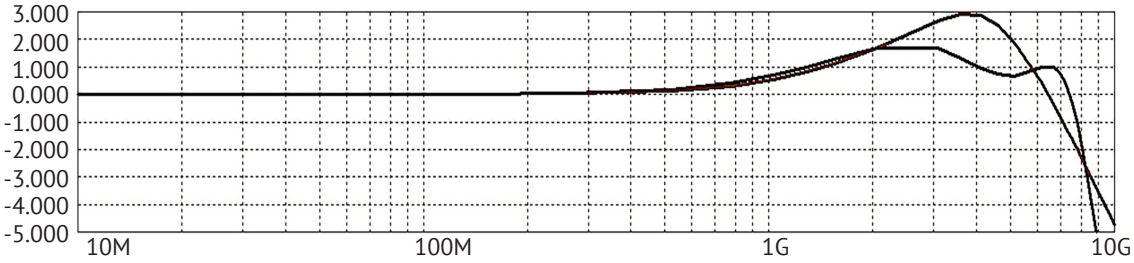

Figure 5. Amplitude-frequency characteristics of a simple and improved buffer device
Source: developed by the authors as a result of modelling in Micro Cap

The implemented precision buffer amplifier, based on a push-pull symmetrical structure, has the following parameters: input signal range: ± 5V; output current: ± 5 mA; zero offset distortion; scale distortion; linearity distortion. Therefore, optimising the amplitude-frequency characteristics was an important step in creating highly efficient voltage buffers, especially for devices that operate in broadband ranges and require high linearity. Ensuring stable signal transmission with minimal distortion is critical for achieving high accuracy and reliability in analogue circuits. The choice of buffer amplifier topology, such as push-pull symmetrical structures, reduces the level of nonlinear distortion, reduces scale and zero offset distortions, and provides a wide range of operating signals. This makes such solutions optimal for use in high-precision measurement systems, analogue-to-digital conversion devices, and other high-speed analogue applications where signal transmission accuracy, energy efficiency, and stable operation under high loads are critical.

In electronic systems, buffer devices perform an important function by ensuring signal consistency between different circuit components, reducing distortion and ensuring stable operation of both analogue and digital devices. Between 2000 and 2020, significant research was conducted to improve buffer cascades, in particular to improve their linearity, expand their bandwidth, and increase their load capacity. One of the main areas of application for buffer devices is analogue-to-digital and digital-to-analogue converters, which are an integral part of modern electronic systems, performing the function of communication between analogue physical quantities and digital computing systems. The work of P. Horowitz & W. Hill (1981) covered a wide range of issues related to the principles of operation, characteristics and practical application of these devices. The authors emphasised that signal conversion systems are used in measuring instruments, communication devices, image processing and other high-precision fields. The works of B. Cordell (2010) and P.E. Allen & D.R. Holberg (2011) included an analysis of the main types of analogue-to-digital and digital-to-analogue converters, the features of their interaction with microprocessor systems, and described typical application circuits – from simple elements to integrated data acquisition systems. Special attention was paid to testing methods and converter specifications, which are critical for their correct integration into practical solutions. In addition, the work considered specialised forms of converters, such as video converters, devices for synchronous and resolver systems, as well as voltage-to-frequency converters. Much attention was also focused on auxiliary components, in particular analogue reference sources, multiplexers and switches, which are important for improving the accuracy and speed of circuits.

The textbook by T.C. Carusone *et al.* (2011) discussed the principles of designing analogue integrated

circuits, in particular buffer amplifiers. The authors have analysed in detail the methods for achieving high linearity and wide bandwidth, which are key aspects for buffers with increased load capacity. Particular attention was paid to circuit solutions that ensure stable operation under variable load conditions.

The development of integrated circuits has significantly changed traditional approaches to the design of electronic devices, particularly in the field of analogue electronics. In the study by W. Sansen (2007) the key aspects of analogue integrated circuit design were highlighted, focusing on their capabilities, limitations and design philosophy. The author provided practical advice for both analog integrated circuit designers and engineers involved in their integration into complex electronic systems. One of the important points discussed in U. Tietze & C. Schenk (2008) is the impact of integrated circuit technologies on traditional methods of designing analogue devices. The authors emphasised that the development of microprocessors and digital signal processing has led to significant improvements in analogue circuits, especially in areas that actively interact with digital devices. This, in turn, has contributed to the creation of complex integrated systems that combine analogue and digital functions on a single chip, ensuring high performance and signal processing accuracy. The study also highlighted the basic principles of analogue integrated circuit design, including methods for reducing distortion and improving linearity and stability. The technological limitations of analogue microcircuit manufacturing were considered separately, as well as the trade-offs between performance, power consumption and chip area.

The book by A.H.M. Roermund *et al*. (2010) contained a collection of modern approaches to the design of analogue circuits, including buffer cascades for high-speed converters. Methods for reducing nonlinear distortions and improving energy efficiency were discussed, which are relevant for the development of buffers with high load capacity. Another key issue in electronic circuit design is reducing delay and power consumption, especially under conditions of heavy load on the output stages. One effective approach to solving this problem is to use bipolar complementary metal-oxide semiconductor buffers, which combine the advantages of bipolar and complementary metal-oxide semiconductor technologies, providing high speed and efficient signal transmission at low supply voltages. The article by M. Kaviani *et al*. (2016) presented bipolar complementary metal-oxide semiconductor buffers operating in the voltage range of 0.8-1.5 V and demonstrating efficient charging and discharging of load capacitors with reduced delay. According to the simulation results, such buffers operate effectively over a wide range of capacitances (0.5-200 pF), making them suitable for circuits with different load levels. The proposed circuits reduced delay by 88% compared to traditional complementary metal-oxide semiconductor buffers at high load capacitance values. It has also been established that bipolar complementary metal-oxide semiconductor buffers have a higher operating frequency range compared to complementary metal-oxide-semiconductor (CMOS) implementations: when the capacitance exceeds 200 pF, the operating frequency of complementary metal-oxide semiconductor buffers decreases by 25% compared to bipolar complementary metal-oxide semiconductor analogues.

The textbook by B. Razavi (2016) provided a detailed description of the design of analogue CMOS integrated circuits, in particular buffer amplifiers. The author analysed methods of linearisation and distortion compensation, which are important for achieving high accuracy and stability of buffers under variable loads. R.J. Baker's (2010) book covered the practical aspects of designing, tracing, and modelling CMOS circuits. It discussed various buffer amplifier topologies, methods for reducing output resistance and improving linearity, which are critical for ensuring high load capacity and wide bandwidth. The publication by M. Fakhfakh *et al*. (2013) presented a systematic approach to the design of analogue and mixed-signal circuits. Particular attention was paid to methods for synthesising buffer amplifiers using only voltage and current repeaters, which contributed to achieving high linearity and wide bandwidth.

One of the directions in the development of broadband high-linearity voltage buffers was to reduce power consumption and increase speed at low operating voltages. A promising solution is the use of heterojunction tunnel transistors, which have a lower subthreshold slope compared to standard metal-oxide-semiconductor field-effect transistors, allowing for significant improvements in energy efficiency even at low power levels (Sharma & Mehra, 2011; Park & Yoo, 2013). The main features of such transistors are asymmetric current and increased Miller capacitance, which creates additional challenges for the design of high-speed circuits. However, the use of heterojunction tunnel transistors in ring generators can significantly reduce dynamic power consumption, and the use of heterojunction tunnel transistors in memory cells can significantly reduce static power losses. These advantages make heterojunction tunnel transistors promising for broadband analogue circuits with high load capacity, where high energy efficiency, low power loss and operational stability are critical.

The book by P. Mak & R.P. Martins (2012) focused on techniques for designing analogue and radio frequency (RF) electronic circuits for nanometre CMOS technologies. Methods for implementing buffer cascades capable of operating at high and mixed voltages were considered, which allowed for high linearity and efficiency under significant loads. Thus, the use of bipolar complementary metal-oxide semiconductor buffers significantly improves the speed of output cascades, reduces delay, and ensures stable operation of circuits at high load levels, making them a promising solution for use

in high-speed analogue-to-digital and digital-to-analogue systems. A review of the literature has shown that the creation of broadband high-linearity buffer devices is an important and relevant task in modern electronics. Research has shown significant progress in improving linearity, expanding bandwidth, and increasing the load capacity of buffer cascades, which is critical for use in high-precision measurement systems, communication devices, and signal processing.

Works related to traditional buffer cascades based on operational amplifiers demonstrated their effectiveness in low-frequency circuits, but bandwidth limitations restrict their use in high-speed conditions. Current research was focused on the development of push-pull high-line structures with parametric compensation, which significantly reduces distortion and improves the metrological characteristics of devices. In addition, the significant impact of digital signal processing and integrated circuits on analogue devices should be noted. Advances in microprocessor technologies have contributed to the improvement of analogue integrated circuit design methods, enabling the creation of complex multifunctional devices that can integrate analogue and digital blocks on a single chip.

CONCLUSIONS

The study considered the proposed approach to constructing a broadband high-linearity voltage buffer with enhanced load-driving capacity, which allows for effective matching of low-power signals with low-impedance loads. The proposed circuit solution was based on the use of cascode and push-pull topologies, which helps to reduce nonlinear distortions, improve stability, and expand the device's bandwidth. A buffer device circuit has been created that meets the increased requirements for load capacity and voltage transfer coefficient. The proposed solution, based on a push-pull symmetrical structure, provides a wide input signal range of ± 5 V and an output current of up to ± 5 mA. During modelling, a low level of zero offset deviation (no more than 1 mV), scale deviation (0.0001%) and linearity deviation (0.000005%) was achieved, which indicates high signal transmission accuracy.

A comprehensive analysis of the static and dynamic characteristics of the buffer cascade was carried out using modern simulation software such as Micro Cap. The influence of transistor element parameters on the stability of the device was investigated, in particular the influence of load resistance on signal transmission linearity. As shown in Table 1, the circuit with an amplifier cascade demonstrates a consistently low level of linearity error even with significant reductions in load resistance, ranging from 12.32 μV to 13.63 μV, whereas without an amplifier, this figure increases sharply to 697.93 μV at a load of 1 kOhm. This improvement is critical for stable device operation in high-load applications.

A comparison of the proposed solution with traditional buffer cascades demonstrated its significant advantages, including reduced harmonic distortion, increased signal transmission accuracy, and significantly better load capacity. This allows the developed solution to be used in high-precision measurement systems, analogue-to-digital converters and amplifiers, where high accuracy and minimal power loss are critical. This is a physical parameter that characterises the effect of temperature on the operation of semiconductor components, in particular transistors. It plays a key role in the formation of current in the p-n junctions of transistors and determines the dependence of the electrical characteristics of the buffer on temperature. This makes the developed device promising for use in high-precision measurement systems, analogue and mixed signal processing circuits, as well as in powerful drivers for controlling low-impedance loads.

The proposed approach to the construction of buffer devices can be applied in analogue-to-digital and digital-to-analogue conversion systems, where high linearity, wide bandwidth and minimal non-linear distortion are critical. Possible areas of application for the developed device have been identified, in particular in high-precision measurement systems, analogue signal processing circuits, and powerful drivers for load control. Further research should be aimed at optimising the design of buffer devices to achieve high linearity, wide bandwidth and low output resistance, which will ensure their effective integration into modern electronic systems.

ACKNOWLEDGEMENTS

None.

FUNDING

None.

CONFLICT OF INTEREST

None.

REFERENCES

[1] Allen, P.E., & Holberg, D.R. (2011). *CMOS analog circuit design*. Oxford: Oxford University Press.
[2] Azarov, O.D., & Stahov, O.Y. (2022). Push-pull voltage buffer devices on bipolar transistors. *Herald of Khmelnytskyi National University: Technical Sciences*, 1(4), 18-22. doi: 10.31891/2307-5732-2022-311-4-18-22.
[3] Baker, R.J. (2010). *CMOS: Circuit design, layout, and simulation*. Piscataway: IEEE Press. doi:10.1002/9780470891179.
[4] Carusone, T.C., Johns, D.A., & Martin, K.W. (2011). *Analog integrated circuit design* (2nd ed.). Hoboken: John Wiley & Sons, Inc.
[5] Chang, A., & Kong, B. (2020). High-speed rail-to-rail class-ab buffer amplifier with compact, adaptive biasing for FPD applications. *Electronics*, 9(12), article number 2018. doi: 10.3390/electronics9122018.

[6] Cordell, B. (2010). *Designing audio power amplifiers*. New York: McGraw-Hill Education.
[7] Fakhfakh, M., Tlelo-Cuautle, E., & Castro-López, R. (2013). *Analog/RF and mixed-signal circuit systematic design*. Berlin: Springer. doi: 10.1007/978-3-642-36329-0.
[8] Horowitz, P., & Hill, W. (1981). The art of electronics. *Physics*, 34(3), 67-71. doi: 10.1063/1.2914480.
[9] Kaviani, M., Sharifi, H., Dolatshahi, M., & Navi, K. (2016). Design of low voltage and high-speed bicmos buffer for driving large load capacitor. *International Journal of Engineering and Manufacturing*, 6(1), 1-9. doi: 10.5815/ijem.2016.01.01.
[10] Kim, S.K., Son, Y.-S., & Cho, G.H. (2006). Low-power high-slew-rate CMOS buffer amplifier for flat panel display drivers. *Electronics Letters*, 4(42), 214-215. doi: 10.1049/el:20063898.
[11] Liao, J., Li, P., Gao, Z., Zhi, Y., Fang, Z., & Zhuang, X. (2025). A low noise differential charge amplifier with input buffer stage for toroidal gyroscope. *Measurement Science and Technology*, 36(5), article number 055112. doi: 10.1088/1361-6501/add314.
[12] Mak, P., & Martins, R.P. (2012). *High-/mixed-voltage analog and RF circuit techniques for nanoscale CMOS*. New York: Springer. doi: 10.1007/978-1-4419-9539-1.
[13] Mythry, S., & Moni, J. (2019). A bulk-driven, buffer-biased, gain-boosted amplifier for biomedical signal enhancement. *Cogent Engineering*, 6(1), article number 1658966. doi: 10.1080/23311916.2019.1658966.
[14] Park, H., & Yoo, C. (2013). Effect of buffer cache on storage performance in virtualised environment. *Electronics Letters*, 4(49), 251-253. doi: 10.1049/el.2012.4069.
[15] Patent No. 158284. (2025). *Buffer cascade*. Retrieved from https://iprop-ua.com/inv/ec9yoxmd/.
[16] Razavi, B. (2016). *Design of analog CMOS integrated circuits* (2nd ed.). New York: McGraw-Hill Education.
[17] Roermund, A.H.M., Casier, H., & Steyaert M. (2010). *Analog circuit design: Smart data converters, filters on chip, multimode transmitters*. Dordrecht: Springer. doi: 10.1007/978-90-481-3083-2.
[18] Rohde, U.L., & Newkirk, D.P. (2000). *RF/microwave circuit design for wireless communications*. New York: John Wiley & Sons, Inc.
[19] Sansen, W. (2007). *Analog design essentials*. London: Springer. doi: 10.1007/b135984.
[20] Sharma, D., & Mehra, R. (2011). Low power, delay optimized buffer design using 70nm CMOS technology. *International Journal of Computer Applications*, 22(3), 13-18. doi: 10.5120/2565-3526.
[21] Tietze, U., & Schenk, C. (2008). *Electronic circuits: Handbook for design and applications*. Berlin: Springer. doi: 10.1007/978-3-540-78655-9.
[22] Yang, B., Caldwell, T., & Chan Carusone, A. (2025). An energy-efficient pipeline-sar ADC using linearized dynamic amplifiers and input buffer in 22nm FDSOI. *IEEE Open Journal of Circuits and Systems*, 6, 50-62. doi: 10.1109/OJCAS.2024.3509746.

Широкосмуговий високолінійний буфер напруги з підвищеною навантажувальною здатністю

Олексій Азаров

Доктор технічних наук, професор
Вінницький національний технічний університет
21021, вул. Хмельницьке шосе, 95, м. Вінниця, Україна
https://orcid.org/0000-0002-8501-1379

Сергій Богомолов

Кандидат технічних наук, доцент
Вінницький національний технічний університет
21021, вул. Хмельницьке шосе, 95, м. Вінниця, Україна
https://orcid.org/0009-0003-3823-8380

Олександр Лукашук

Аспірант
Вінницький національний технічний університет
21021, вул. Хмельницьке шосе, 95, м. Вінниця, Україна
https://orcid.org/0009-0002-7485-1193

Анотація. Розробка буферних каскадів із високою лінійністю, широкою смугою пропускання та здатністю працювати з низькоомним або ємнісним навантаженням є актуальним завданням сучасної аналогової електроніки. Метою цієї роботи було створення широкосмугового високолінійного буфера напруги з підвищеною навантажувальною здатністю для застосування у високоточних системах. У дослідженні використано метод комп'ютерного моделювання для аналізу електричних параметрів запропонованого каскаду, а також проведено порівняння з традиційними схемами. Запропоновано новий схемотехнічний підхід до побудови буферного каскаду, що базується на оптимізованій структурі вихідного етапу та поєднанні каскодної і двотактної топологій. Така конфігурація дозволяє знизити вихідний опір, зменшити нелінійні викривлення і забезпечити високу стабільність передачі сигналу. Результати моделювання підтвердили, що розроблений буфер має розширену смугу пропускання, покращені частотні характеристики та знижене гармонічне спотворення в широкому діапазоні частот. Зокрема, під час роботи з навантаженнями великої ємності (до 200 пФ) спостерігалося суттєве зниження затримки сигналу (до 80-90 %) у порівнянні зі звичайними комплементарними структурами метал-оксид-напівпровідник реалізаціями. Оцінка впливу параметрів активних елементів на динамічну стабільність роботи також засвідчила високу надійність пристрою в умовах змінного навантаження. Результати дослідження можуть бути використані для покращення продуктивності аналогово-цифрових перетворювачів, драйверів, підсилювачів і схем керування, що працюють у режимах із підвищеним струмовим навантаженням. Практична цінність розробки полягає в можливості її інтеграції у високоточні, енергоефективні та швидкодійні електронні системи, що потребують стабільної роботи буферного каскаду за складних умов навантаження

Ключові слова: високонавантаженість; високоточність; буферний пристрій; каскодний каскад; двотактна структура